

REMARKS

Claims pending in the present patent application are numbered 1, 3 and 6-8. Claims 2, 4, 5 and 9-15 are canceled herein without prejudice. Claims 1 and 3 are amended herein. No new matter has been added as a result of these claim amendments. The rejections set forth in the Office Action dated December 23, 2005, have been carefully considered by the Applicant. Examiner's rejections are respectfully traversed below. Applicants respectfully assert that the pending Claims are in condition for allowance.

RESPONSES TO CLAIM REJECTIONS

35 USC § 102

Claims 1-4, 6-11 and 13-15 are rejected under 35 U.S.C. 102 as being anticipated by Tanaka (US Patent No. 6,756,675; hereinafter "Tanaka"). Claims 2, 4, 9-11 and 13-15 are canceled herein. Applicants respectfully traverse the rejection of Claims 1, 3 and 6-8.

Claim 1 recites:

A semiconductor device comprising:
a pad metal layer having a perimeter area and a center area;
a lower metal layer having a plurality of apertures below said center area of said pad metal layer, wherein said apertures are arranged into a plurality of rows each row comprising more than one of said apertures and a plurality of columns each column comprising more than one of said apertures;
an interlayer dielectric formed between said pad metal layer and said lower metal layer;
a plurality of vias formed in said interlayer dielectric, wherein said vias electrically couple said pad metal layer and said lower metal layer, and wherein said vias form a ring arrangement only below said perimeter area of said pad metal layer; and

an insulating dielectric layer that covers said perimeter area of said pad metal layer. (emphasis added)

In Figures 1-9B and the corresponding text, Tanaka teaches a semiconductor device having a pad metal layer **100** over a lower pad metal layer **200**, wherein the lower metal layer **200** has a plurality of apertures **130a-130g**. Tanaka teaches an insulating layer **150** between the pad **100** and lower **200** metal layers. Tanaka also teaches a plurality of vias **110a-120d** connecting the pad **100** and lower **200** metal layers.

However, In Figures 1, 2A, 6A, 7A, 8 and 9A Tanaka teaches that the plurality of vias connecting the pad **100** and lower **200** metal layers are positioned throughout the insulating layer **150**. In contrast, Claim 1 recites “a plurality of vias formed in said interlayer dielectric, wherein said vias electrically couple said pad metal layer and said lower metal layer, and wherein said vias form a ring arrangement **only below said perimeter area** of said pad metal layer.” Tanaka fails to teach or suggest the ring arrangement of vias located only below the perimeter area recited in Claim 1.

Tanaka also fails to teach or suggest the “insulating dielectric layer that covers said perimeter area of said pad metal layer” recited in Claim 1. Applicants respectfully traverse Examiner’s rejection of Claim 1 under 35 U.S.C. 102 as being anticipated by Tanaka. Applicants respectfully assert that Claim 1 is in condition for allowance. Claims 3 and 6-8 are dependent on Claim 1 and recite further limitations, therefore Applicants respectfully traverse Examiner’s rejection of Claims 3 and 6-8 under 35 U.S.C. 102 as being anticipated by Tanaka, and respectfully assert that Claims 3 and 6-8 are also in condition for allowance.

35 USC § 103

Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Heim (U.S. Patent No. 5,248,903; hereinafter "Heim"). Claims 5 and 12 are canceled herein.

CONCLUSION


It is respectfully submitted that the above claims, arguments and remarks overcome all rejections. All remaining claims (Claims 1, 3 and 6-8) are neither anticipated by nor obvious in view of the cited references. For at least the above-presented reasons, it is respectfully submitted that all remaining claims (Claims 1, 3 and 6-8) are in condition for allowance.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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